IN THE CLAIMS

Please amend the claims as follows:

Claims 1-12 (Canceled).

Claim 13 (Currently Amended): A silicon carbide semiconductor device, comprising:

a lower deposition film which is formed of a single layer of silicon carbide of a first conductivity type, and which has lower impurity concentration than a high impurity concentration silicon carbide substrate of the first conductivity type and which is formed on a surface of the silicon carbide substrate;

a high impurity concentration gate region of a second conductivity type selectively formed across from an upper surface to an interior of the lower deposition film, the high impurity concentration gate region being adjacent to and in contact with a non-implanted portion that is an exposed part of the upper surface of the lower deposition film;

an upper deposition film formed on the lower deposition film in which the high impurity concentration gate region is formed, wherein the upper deposition film comprises: a low impurity concentration gate region of the second conductivity type directly deposited on a surface of the high impurity concentration gate region of the second conductivity type and having a lower impurity concentration than the high impurity concentration gate region; a high impurity concentration source region of the first conductivity type selectively formed on part of an upper surface of the low impurity concentration gate region of the second conductivity type and being more heavily doped than the low impurity concentration gate region of the second conductivity type; and a low impurity concentration base region of the first conductivity type formed on the non-implanted portion and having a greater width than the non-implanted portion and being doped less than the high impurity concentration source region of the first conductivity type;

a gate insulation film formed on at least a surface of the upper deposition film;

a gate electrode formed via the gate insulation film;

a drain electrode having a low-resistance contact connection with a backside of the silicon carbide substrate of the first conductivity type; and

a source electrode having a low-resistance contact connection with part of the high impurity concentration source region of the first conductivity type and the low impurity concentration gate region of the second conductivity type.

Claim 14 (Currently Amended): A silicon carbide semiconductor device according to claim 13, wherein the upper deposition film has a thickness within a range of 0.2 μm to 0.7 μm and wherein the low impurity concentration gate region of the second conductivity type selectively formed in the upper deposition film has a portion that is in contact with the gate insulation film and has an impurity impurity concentration higher than 1×10^{15} cm^{-3} and lower than 5×10^{15} cm^{-3}.

Claim 15 (Currently Amended): A silicon carbide semiconductor device according to claim 13, wherein the low impurity concentration base region of the first conductivity type has a lower impurity concentration than the high impurity concentration gate region of the second conductivity type.

Claim 16 (Currently Amended): A silicon carbide semiconductor device according to claim 13, wherein the low impurity concentration gate region of the second conductivity type selectively formed in the upper deposition film has a portion that is in contact with the gate insulation film and has an impurity concentration of not higher than 2×10^{16} cm^{-3}.

Claim 17 (Previously Presented): A silicon carbide semiconductor device according to claim 13, wherein the upper deposition film is constituted of silicon carbide.

Claim 18 (Withdrawn/Currently Amended): A silicon carbide semiconductor device according to claim 13, wherein the gate insulation film formed on the upper deposition film has at least a portion that is thicker than other portions on the low impurity concentration base region of the first conductivity type selectively formed in the upper deposition film.

Claim 19 (Withdrawn/Previously Presented): A silicon carbide semiconductor device according to claim 13, wherein on the surface of the base region of the first conductivity type selectively formed in the upper deposition film, the gate electrode has at least a portion removed.

Claim 20 (Previously Presented): A silicon carbide semiconductor device according to claim 13, wherein in terms of crystal Miller index the surface of the silicon carbide substrate of the first conductivity type is a plane that is parallel to a (11-20) plane.

Claim 21 (Previously Presented): A silicon carbide semiconductor device according to claim 13, wherein in terms of crystal Miller index the surface of the silicon carbide substrate of the first conductivity type is a plane that is parallel to a (000-1) plane.

Claim 22 (Withdrawn/Currently Amended): A silicon carbide semiconductor device according to claim 13, wherein the low impurity concentration gate region of the second conductivity type has a portion that is in contact with the gate insulation film and has a buried channel region of the first conductivity type.

Claims 23-26 (Canceled).

Claim 27 (Currently Amended): A silicon carbide semiconductor device according to claim 13, wherein

high impurity concentration gate regions including the high impurity concentration gate region of the second conductivity type are formed on both sides of the non-implanted portion so that the non-implanted portion will be formed in an intermediate part of [[an]] the upper surface of the lower deposition film,

[[low]] high concentration gate regions including the high impurity concentration gate region of the second conductivity type are respectively directly deposited on surfaces of the high impurity concentration gate regions of the second conductivity type on both sides of the base region of the first conductivity type, and

source regions including the source region of the first conductivity type are respectively formed on parts of upper surfaces of the low impurity concentration gate regions of the second conductivity type on both sides of the base region of the first conductivity type.